WHAT IS CLAIMED IS:

1. A PLL circuit for receiving either one of first and second reference signals to generate a clock signal synchronized with one of the first and second reference signals, wherein the first reference signal is generated by superimposing a first wobble signal having a first cycle on a land pre-pit signal, and the second reference signal is generated from a second wobble signal having a second cycle shorter than the first cycle, the PLL circuit comprising:

a voltage-controlled oscillator for generating the clock signal in accordance with control voltages;

a first loop, connected to the voltage-controlled oscillator, for controlling at least one of a frequency and a phase of the clock signal in accordance with one of the first wobble signal and the second wobble signal;

a second loop, connected to the voltage-controlled oscillator, for controlling at least one of the frequency and the phase of the clock signal in accordance with the land pre-pit signal, wherein the first and second loops are validated when the PLL circuit is provided with the first reference signal, and the first loop is validated and the second loop is invalidated when the PLL circuit is provided with the second reference signal.

2. The PLL circuit according to claim 1, wherein the second loop supplies the voltage-controlled oscillator with control voltage in accordance with a phase difference between the first reference signal and the clock signal when the PLL circuit is provided with the first reference signal, and the second loop supplies the voltage-controlled oscillator with constant control voltage when the PLL circuit is provided with the second reference signal.

3. The PLL circuit according to claim 2, further comprising:

a voltage generation circuit for generating the constant voltage; and

a switching circuit, connected between the voltage generation circuit and the second loop, for connecting the voltage generation circuit to the second loop when the PLL circuit is provided with the second reference signal and for disconnecting the voltage generation circuit from the second loop when the PLL circuit is provided with the first reference signal.

4. The PLL circuit according to claim 1, wherein the first loop includes:

a phase comparator for outputting a phase difference signal that is in accordance with one of a phase difference between the first wobble signal and the clock signal and a phase difference between the second wobble signal and the clock signal; and

a charge pump for generating a controlled output current in accordance with the phase difference signal, the charge pump having a variable gain.

5. The PLL circuit according to claim 4, wherein the charge pump includes:

a plurality of charge pump units; and

a gain switching circuit for selectively driving the charge pump units in accordance with the phase difference signal, the gain switching circuit changing the number of the charge pump units that are driven to vary the gain of the charge pump.

6. The PLL circuit according to claim 1, further comprising:

a divider for dividing at least one of the first wobble signal, the second wobble signal, and the clock signal, the divider having a dividing ratio that differs when the PLL circuit is provided with the first reference signal and when the PLL circuit is provided with the second reference signal.

7. The PLL circuit according to claim 1, wherein the voltage-controlled oscillator variably alters the rate of change of at least one of the frequency and the phase of the clock signal relative to the control voltages.

8. The PLL circuit according to claim 1, wherein the voltage-controlled oscillator includes:

a first input terminal connected to the first loop and supplied with control voltage from the first loop in accordance with one of the phase difference between the first wobble signal and the clock signal and the phase difference between the second wobble signal and the clock signal;

a second input terminal connected to the second loop and supplied with control voltage from the second loop in accordance with the phase difference between the land pre-pit signal and the clock signal; and

a ring oscillator for generating an oscillation output signal in accordance with the control voltages applied to the first and second input terminals.

9. A PLL circuit for generating a clock signal from a first wobble signal having a first cycle and a land pre-pit signal or from a second wobble signal having a second cycle shorter than the first cycle, the PLL circuit comprising:

a voltage-controlled oscillator including a first input terminal and a second input terminal respectively receiving a first control voltage and a second control voltage for generating the clock signal with a frequency and a phase that

are in accordance with the first and second control voltages;

a first loop, connected to the voltage-controlled oscillator, including a first divider for dividing the clock signal to generate a first divisional clock signal and a frequency comparator, connected to the first divider, for comparing the frequency of one of the first wobble signal and the second wobble signal with the frequency of the first divisional clock signal, the first loop generating the first control voltage in accordance with the frequency difference between the two compared signals;

a second loop, connected to the voltage-controlled oscillator, including a second divider for dividing the clock signal to generate a second divisional clock signal and a phase comparator, connected to the second divider, for comparing the phase of the land pre-pit signal and the phase of the second divisional clock signal, the second loop generating the second control voltage in accordance with the phase difference between the two compared signals, and the voltage-controlled oscillator being shared by the first and second loops; and

a voltage generation circuit for generating a constant voltage;

wherein the first and second input terminals are respectively supplied with the first and second control voltages when the PLL circuit is provided with the first wobble signal and the land pre-pit signal, and the first and second input terminals are respectively supplied with the first control voltage and the constant voltage and the second control voltage is invalidated when the PLL circuit is provided with the second wobble signal.

10. The PLL circuit according to claim 9, wherein the first divider divides the clock signal with a first dividing ratio when the PLL circuit is provided with the first wobble

signal, and the second divider divides the clock signal with a second dividing ratio, which differs from the first dividing ratio, when the PLL circuit is provided with the second wobble signal.

11. The PLL circuit according to claim 9, further comprising:

a switching circuit, connected between the voltage generation circuit and the second loop, for connecting the voltage generation circuit to the second loop when the PLL circuit is provided with the second wobble signal and for disconnecting the voltage generation circuit from the second loop when the PLL circuit is provided with the first wobble signal and the land pre-pit signal.